Simulation of a SVPWM Applied to a Buck –Boost Voltage Source Two Level Inverter

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Abstract: This paper presents successful application of a space vector pulse width amplitude modulation (SVPWAM) for buck –boost voltage source inverter. It is a standard PWM technique to utilize the DC-AC power conversion, for a voltage source inverter, in this technique the switching losses is reduced by 87%, as compared to conventional sinusoidal pulse width amplitude modulation (SPWM) method. In this case power density increased by a factor of 2 to 3. In addition, it is also verified that the output harmonic distortions of SVPWAM is lower than SPWM. The switching power loss is reduced by 90% compared with the conventional SPWM inverter system. Hence to obtain the good voltage transfer and reduced switching losses SVPWAM is used. As a result, SVPWAM is used to make the buck–boost inverter suitable for applications that require high efficiency, high power density, high temperature, and low cost, such as EV motor drive or engine starter/synchronous machines. In this work, a buck boost voltage source inverter using space vector modulation strategy has been modeled and simulated. Simulation results are obtained using MATLAB/Simulink environment for effectiveness of the study.

Index Terms: Buck-boost, SVPWAM, THD, Inverter

I. INTRODUCTION

Space Vector PWM (SVPWM) is a more sophisticated technique for generating a fundamental sine wave that provides a higher voltage and lower total harmonic distortion (THD) and reduced switching losses.
Fig. 1 shows a typical configuration of the series plug-in electric vehicle (PHEV). The inverter is required to inject low harmonic current to the motor, in order to reduce the winding loss and iron loss. For this purpose, the switching frequency of the voltage source inverter is designed within a high range from 15 to 20 kHz, resulting in the switching loss increase in switching device and also the iron loss increase in the motor stator. To solve this problem, various soft-switching methods have been proposed [1]–[3].

This paper proposes a space vector pulse width amplitude modulation (SVPWAM) method for the buck/boost voltage source inverter (VSI). By eliminating the conventional zero vector in the space vector modulation, two-third switching frequency reduction can be obtained in VSI. If a unity power factor is assumed, an 87% switching loss reduction can be implemented in VSI, The Space Vector Pulse Width Modulation (SVPWM) refers to a special switching sequence of the power devices of a buck-boost voltage source inverters (VSI) used in application such as electric motor drive and synchronous generator. Space Vector PWM (SVPWM) method is an advanced; and possibly the best techniques for variable frequency drive application. SVPWM generates less harmonic distortion in the output voltages and currents in the windings of the motor load and provides a more efficient use of the DC supply voltage in comparison with sinusoidal modulation techniques. Although SVPWM is more complicated than sinusoidal PWM, it may be implemented easily with modern DSP based control systems. In Space vector Modulation (SVPWM) we consider a rotating phased which is obtained by adding all the three voltages. Modulation is accomplished by switching state of an inverter.
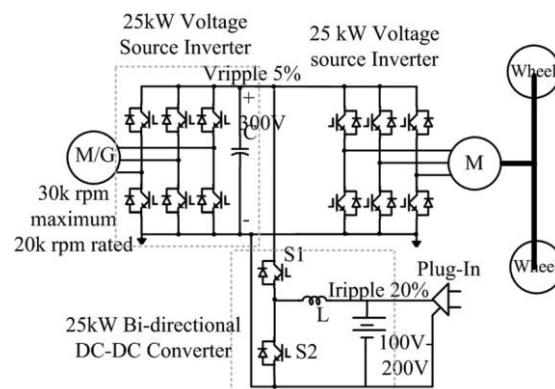

Fig.1 Typical configuration of a series PHEV.

Buck-boost inverters have the advantage of converting dc voltage higher or lower than the utility voltage without utilizing a line frequency transformer [4]. Two stage or multiple stage configurations are commonly used in buck-boost inverters. Such inverter systems have dc-dc or dc-ac-dc converters added to obtain an elevated dc voltage ahead of inversion. A two-stage buck-boost inverter can achieve a relatively high power capacity; nevertheless, the additional power stage requires more power components and thus higher costs.

II. SVPWAM FOR VSI

A. *principal of SVPWAM control in VSI*

The principle of an SVPWAM control is to eliminating the zero vectors in each sector. A different approach to SPWM is based on the space vector representation of voltages in the d, q plane. The d, q components are found by Park transform, where the total power, as well as the impedance, remains unchanged. Fig. 2 shows 8 space vectors in according to 8 switching positions of inverter, V* is the phase-to-center voltage which is obtained by proper selection of adjacent vectors V1 and V2. The reference space vector V* is given by Equation (1), where T1, T2 are the intervals of application of vector V1 and V2 respectively, and zero vectors V0 and V7 are selected for T0. The modulation principle of SVPWAM is shown in Fig.3 and decomposition of voltage vector shown in Fig.4

$$V^* \ Tz = V1 \ ^*T1 + V2 \ ^*T2 + V0 \ ^*(T0/2) + V7 \ ^*(T0/2) \qquad (1)$$
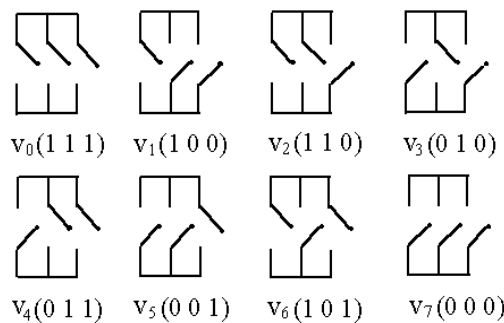

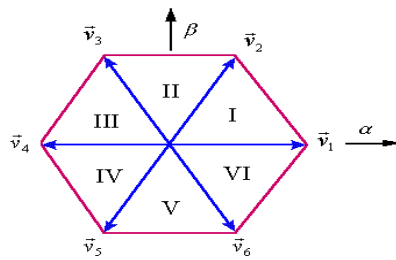**Fig.2.** The switching configurations of a 3-phase PWM inverter
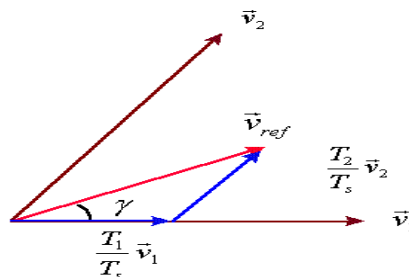

Fig.3. The corresponding vectors.

Fig.4 The decomposition of the voltage vector

In each sector, only one phase leg is doing PWM switching; thus, the switching frequency is reduced by two-third. This imposes zero switching for one phase leg in the adjacent two sectors. For example, in sector VI and I, phase leg A has no switching at all. The dc-link voltage thus is directly generated from the output line-to-

line voltage. In sector I, no zero vectors are selected. Therefore, *S*1 and *S*2 keep constant ON, and *S*3 and *S*6 are doing PWM switching. As a result, if the output voltage is kept at the normal three-phase sinusoidal voltage, the dc-link voltage should be equal to line-to-line voltage *V*ac at this time [5].
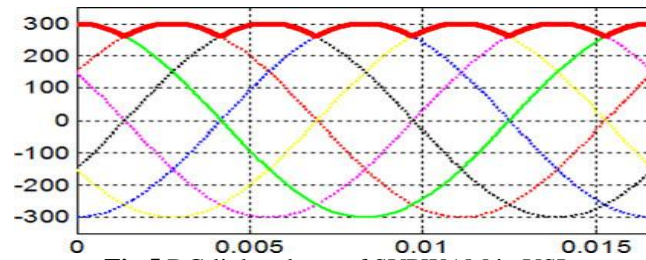

Fig.5 DC-link voltage of SVPWAM in VSI

Consequently, the dc-link voltage should present a 6ω varied feature to maintain a desired output voltage. The corresponding waveform is shown in solid line in Fig. 5. A dc–dc conversion is needed in the front stage to generate this 6ω voltage. The original equations for time period *T*1 and *T*2 are

$$T_1 = \frac{\sqrt{3}}{2}m \sin(60=\phi) \; ; \; T_2 = \frac{\sqrt{3}}{2}m \sin(\phi) \qquad (1)$$

where $\theta \in [0, \pi/3]$ is relative angle from the output voltage Vector to the first adjacent basic voltage vector like in Fig. 3. If the time period for each vector maintains the same, the switching frequency will vary with angle, which results in a variable inductor current ripple and multi frequency output harmonics. Therefore, in order to keep the switching period constant but still keep the same pulse width as the original one, the new time periods can be calculated as

$$T1/Ts = T1/(T1 + T2) \qquad (2)$$

PWM gating signals of the SVPWM operating at each section shown in Fig. 6 Fig. 7 shows the output line-to-line
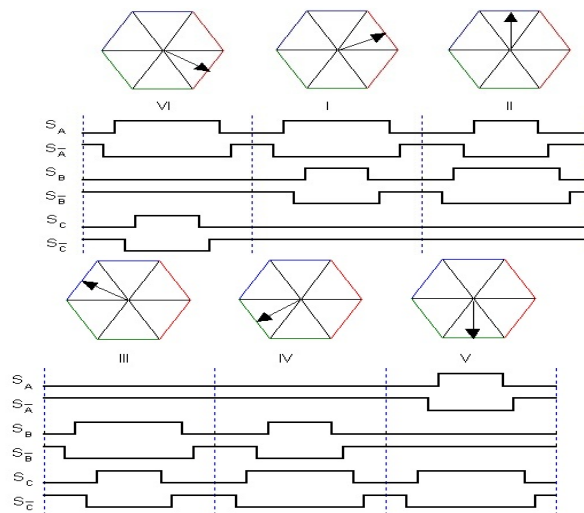
Voltage and the switching signals of *S*1 .

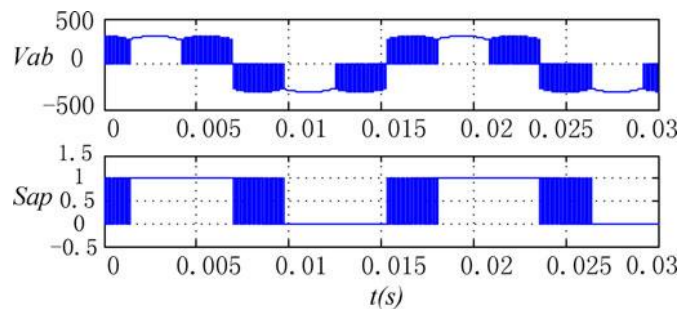**Fig.6.** PWM gating signals of the SVPWM operating at each section

Fig. 7 Theoretic waveforms of dc-link voltage, output line–to-line voltage and switching signals.

B. *Inverter Switching Loss Reduction for VSI*

For unity power factor case, the inverter switching loss is reduced by 87% because the voltage phase for PWM switching is within $[-60°, 60°]$, at which the current is in the zero-crossing region. In VSI, the device voltage stress is equal to dc-link voltage V_{DC}, and the current stress is equal to output current ia. Thus the switching loss for each switch is

$$P_{Sw\_1} = \frac{1}{2\pi}\left[\int_{-\pi/6}^{\pi/6} E_{SR} \frac{|I_m \sin(wt).V_{DC}|}{V_{ref} I_{ref}}.f_{sw}\,d\omega t\right.$$
$$\left. +\int_{5\pi/6}^{7\pi/6} E_{SR} \frac{|I_m \sin(wt).V_{DC}|}{V_{ref} I_{ref}}.f_{sw}\,d\omega t\right]$$

$$= \frac{2-\sqrt{3}}{\pi}\frac{I_m V_{DC}}{V_{ref} I_{ref}} E_{SR}.f_{sw}$$

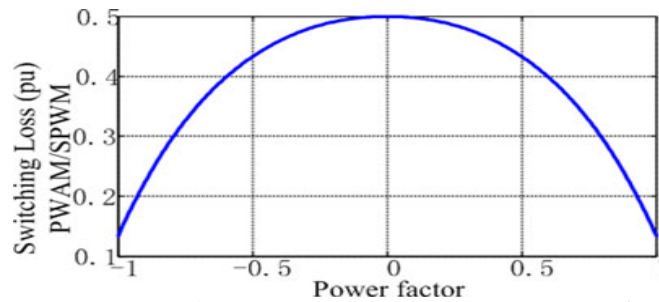where E_{SR}, V_{ref}, I_{ref} are the references

Fig.8. (SVPWAM power loss/SPWM power loss) versus power factor in VSI

Since the SVPWAM only has PWM switching in two 60° sections, the integration over 2π can be narrowed down into integration within two 60°

$P_{SW\_1} = (2\sqrt{3})/\pi.(I_m V_{dc}/V_{ref}I_{ref})).E_{SR}.F_{SW}$ (3)

The switching loss for a conventional SPWM method is

$P_{SW\_1} = (2/\pi).(I_m V_{dc}/V_{ref}I_{ref}))).E_{SR}.F_{SW}$ (4)

In result, the switching loss of SVPWAM over SPWM is $f = 13.4\%$.

However, when the power factor decreases, the switching loss reduction amount decreases because the switching current increases as Fig. 8 shows.

As indicated, the worst case happens when power factor is equal to zero, where the switching loss reduction still reaches 50%. In conclusion, SVPWAM can bring the switching loss down by 50–87%.

C. *Comparison of Sinusoidal PWM and Space Vector PWM*

1) In the Fig. 9 U is the phase-to-center voltage containing the triple order harmonics that are generated by space vector PWM, and U1 is the sinusoidal reference voltage. But the triple order harmonics are not appeared in the phase-to-phase voltage as well. This leads to Modulation Index is higher for SVPWM as compared to SPWM.

2) SPWM only reaches to 78 percent of square-wave operation, but the amplitude of maximum possible voltage is 90 percent of square-wave in the case of space vector PWM. The maximum phase-to-center voltage by sinusoidal and space vector PWM are respectively; **Vmax = Vdc/2** : for Sinusoidal PWM; And **Vmax = Vdc/□3**, where, Vdc is DC-Link voltage: for Space Vector PWM. This means that Space Vector PWM can produce about 15 percent higher than Sinusoidal PWM in output voltage.
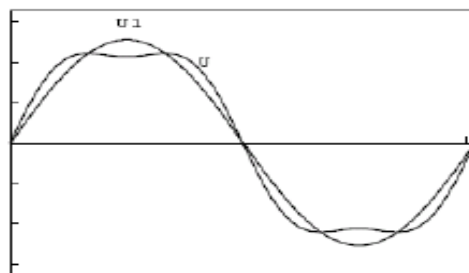

Fig. 9. Phase-to-center voltage by space vector PWM

3) The current and torque harmonics produced are much less in case of SVPWM.
However despite all the above mentioned advantages that SVPWM enjoys over SPWM, SVPWM algorithm used in three-level inverters is more complex because of large number of inverter switching states

III. TOPOLOGIES FOR SVPWAM

Basically, the topologies that can utilize SVPWAM have two stages: dc–dc conversion which converts a dc voltage or current into a 6ω varied dc-link voltage or current; VSI for which SVPWAM is applied. However, the same function can also be implemented in a single stage, such as Z/quasi-Z/trans-Z source inverter [6]–[7].

The front stage can also be integrated with inverter to form a single stage. Take current-fed quasi-Z-source inverter as an example. Instead of controlling the dc-link current I_{pn} to have a constant average value, the open zero state duty cycle D_{op} will be regulated instantaneously to control I_{pm} to have a 6ω fluctuate average value, resulting in a pulse type 6ω waveform at the real dc-link current I_{pn}, since I_1 is related to the input dc current I_{in} by a transfer function

$$I_1 = \frac{1-D_{op}}{1-2D_{op}} I_{IN}$$

In summary for voltage-fed switched-coupled-inductor inverter, it is featured as a single-stage buck-boost voltage source inverter with coupled-inductor. Its advantages contain: (1) high boost ratio (2) tolerating shoot-through (3) reduced size. Its disadvantages include: (1) high voltage stress on the device when boost ratio is high (2) clamp circuit is needed because of the leakage inductance of coupled inductor (3) discontinuous input current. However, the first disadvantage can be overcome because different topologies can be selected at different voltage gain requirement to achieve minimum voltage/current stress on devices or passives [8].

IV. IV. CASE STUDY: 1-KWBOOST-CONVERTER INVERTER FOR EV MOTOR DRIVE APPLICATION

A. Basic Control Principle
The circuit schematic and control system for a 1-kW boost-converter inverter motor drive system is shown in Fig. 10.
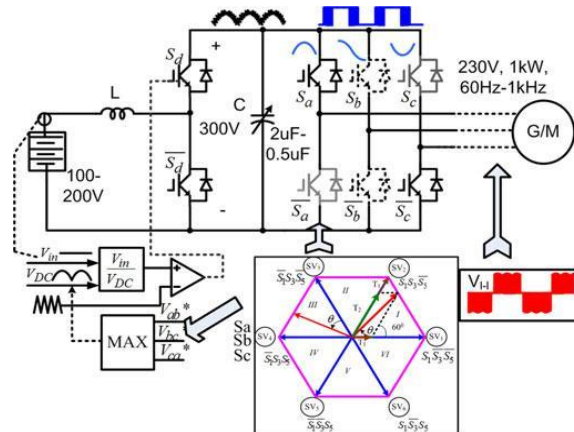

Fig. 10. SVPWAM-based boost-converter-inverter motor drive system

A 6ω dc-link voltage is generated from a constant dc voltage by a boost converter, using open-loop control. Inverter then could be modulated by a SVPWAM method. The specifications for the system are input voltage is 100–200 V; the average dc-link voltage is 300 V; output line-to-line voltage rms is 230 V; and frequency is from 60 Hz to 1 kHz.

B. Voltage Constraint and Operation Region
It is worth noting that the SVPWAM technique can only be applied when the batteries voltage falls into region $V_{in} \leq \sqrt{\frac{3}{2}} V_{l-l}$ due to the step-up nature of boost converter. The constraint is determined by the minimum point of the 6ω dc-link voltage. Beyond this region, conventional SPWM can be implemented. However, the dc-link voltage in this case still varies with 6ω because of the small film capacitor we selected. Thus, a modified SPWM with varying dc-link voltage will be adopted during the motor start up as shown in Fig. 11. Hence, the system will achieve optimum efficiency when the motor is operating a little below or around nominal voltage. When the motor demands a low voltage during start up, efficiency is the same as the conventional SPWM-controlled inverter.
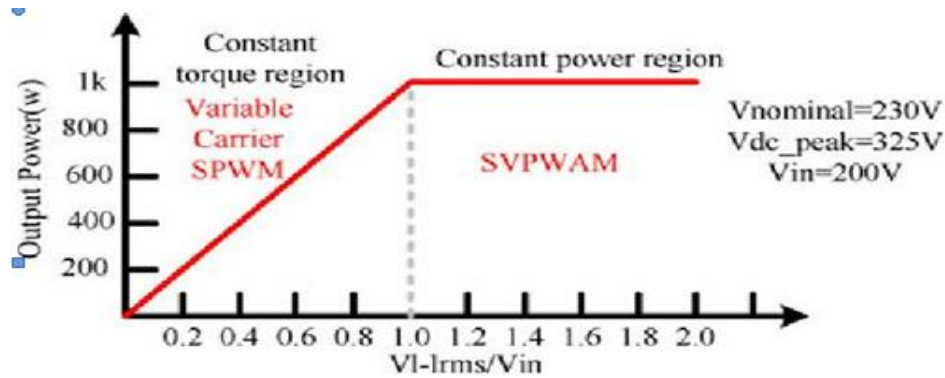
Fig. 11 Operation region of boost-converter-inverter EV traction drive.
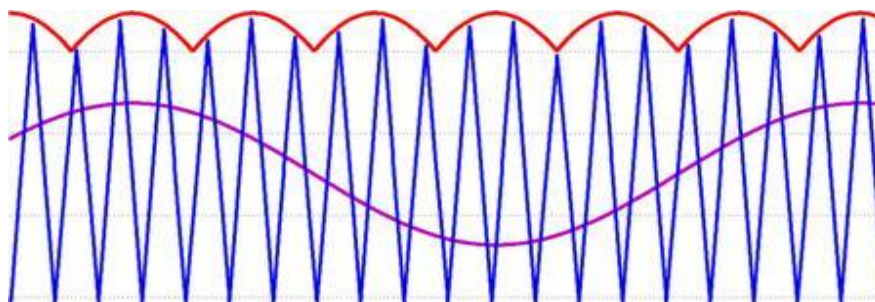

Fig. 12 Variable carrier SPWM control in buck mode

In SVPWAM control of boost mode, dc-link voltage varies with the output voltage, in which the modulation index is always kept maximum. So, when dc-link voltage is above the battery voltage, dc-link voltage level varies with the output voltage. The voltage utilization increased and the total power stress on the devices has been reduced.

C. Variable DC-Link SPWM Control at High Frequency

When the output needs to operate at a relative high frequency, like between 120 Hz and 1 kHz, it is challenging to obtain a 6ω dc-link voltage without increasing the switching frequency of a boost converter. Because the controller does not have enough bandwidth.

Furthermore, increasing boost converter switching frequency would cause a substantial increase of the total switching loss, because it takes up more than 75% of the total switching loss. The reason is because it switches at a complete current region. Also a normal SPWM cannot be used in this range because the capacitor is designed to be small that it cannot hold a constant dc link voltage. Therefore, the optimum option is to control the dc link voltage to be 6ω and do a variable dc link SPWM modulation, as explained in Fig. 12.

In this variable dc-link SPWM control, in order to get bet-ter utilization of the dc-link voltage, an integer times between the dc-link fundamental frequency and output frequency is preferred. When the output frequency is in [60 Hz, 120 Hz], a 6ω dc link is chosen; when the frequency is in [120 Hz, 240 Hz], a 3ω dc link is chosen;

Increases from 0 to full rating under two methods. Since the research target is only inverter, the test condition is based on varying the output power by changing output voltage from 0 to 230 V. It is observed that in the SVPWAM method, conduction loss accounts for 80% of the total power loss, but in the SPWM method, switching loss is higher than conduction loss. The switching loss is reduced from 10 to 1.4 W from SPWM to SVPWAM. An estimated 87% switching loss reduction has been achieved [10].

V. MATLAB MODELING BLOCK DIAGRAM SIMULATION RESULTS

The simulation block diagram of buck –boost voltage source two level inverter shown in below fig.16 in order to get distortion output we are using lp second order filter. Inverter of output of three phases separated into two phases and three phases by providing the one outage block. The buck- boost DC – DC Converter is connected to three phase inverter shown in fig. 17 the SVPWM produces the control signal is given to three phase inverter of MOSFET switches shown in fig.18.
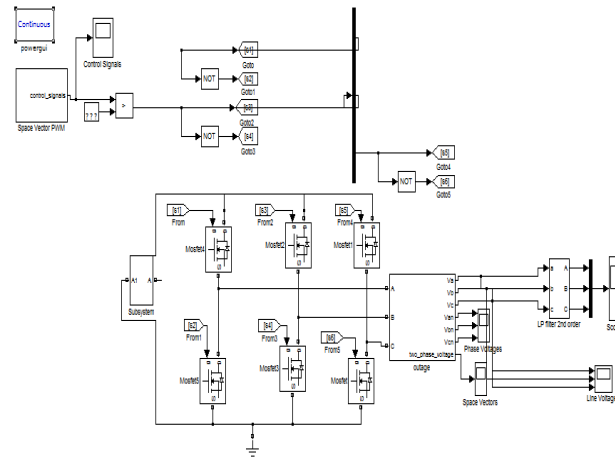
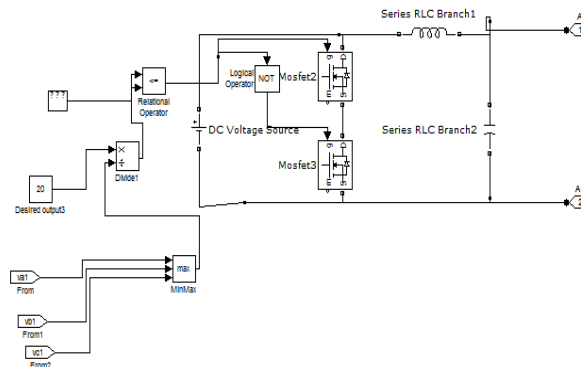**Fig.16** Shows block diagram of buck –boost voltage source two level inverter.

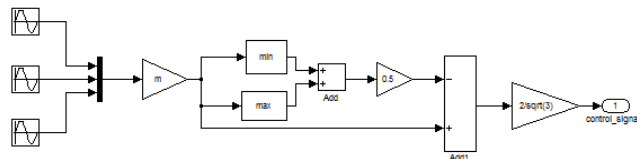**Fig.17** Shows the buck- boost DC – DC Converter

Fig. 18 Shows the control signal of SVPWM

Figs. 19–22 show the output and input voltage, current waveform when input voltage increases from 20 to 100 V, while keeping the boost ratio constant. In this case, the output voltage increases linearly with input voltage increase. The output power increases in proportion to square of the input voltage.

Fig. 19 Presents Simulation results of inverter output line to line voltages (ViAB, ViBC,ViCA)

Fig. 20 Presents Simulation results of inverter output currents (iiA, iiB,iiC)

Fig. 21 Presents Simulation results of filtered line to line voltages (VLAB, VLBC,VLCA)

Fig. 22 Simulation results of load phase currents (iLA, iLB, iLC)

Fig. 23 presents shows Inverter output phase voltage

Fig.24 shows simulation results of switching signals

In short, simulation are identical, they verify that different discontinuous modulation strategies correspond to different un switching intervals, and output voltage of discontinuous modulation strategies is slightly greater than that of continuous modulation.

It is observed that in the SVPWAM method, conduction loss accounts for 80% of the total power loss, but in the PWM method, switching loss is higher than conduction loss. The switching loss is reduced from 10 to 1.4 W from SPWM to SVPWAM. An estimated 87% switching loss reduction has been achieved[11].
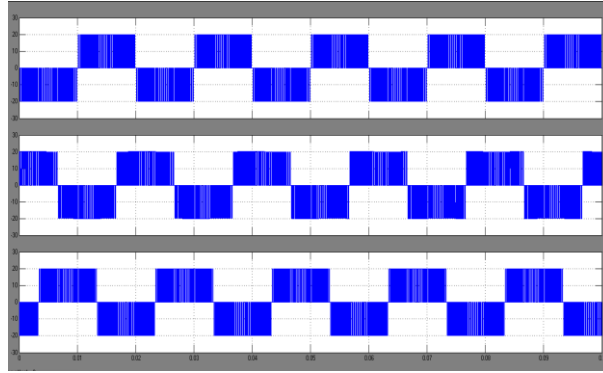
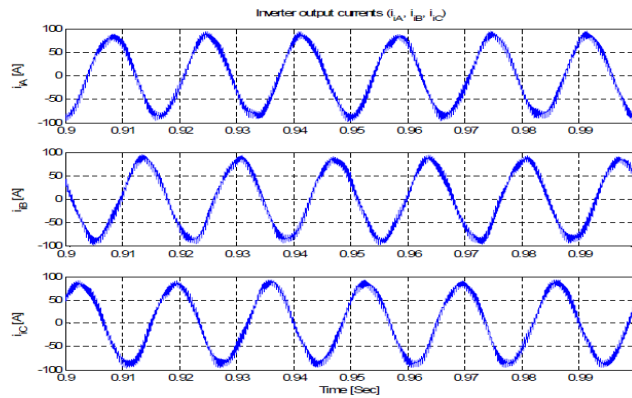**Fig. 19** Simulation results of inverter output line to line voltages (ViAB, ViBC, ViCA)

Fig. 20 Simulation results of inverter output currents (iiA, iiB, iiC)

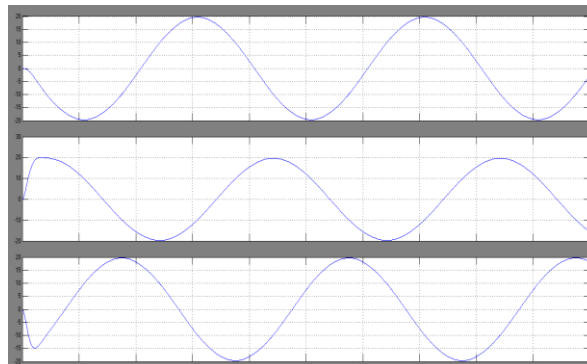**Fig. 21** Simulation results of filtered line to line voltages (VLAB, VLBC, VLCA)

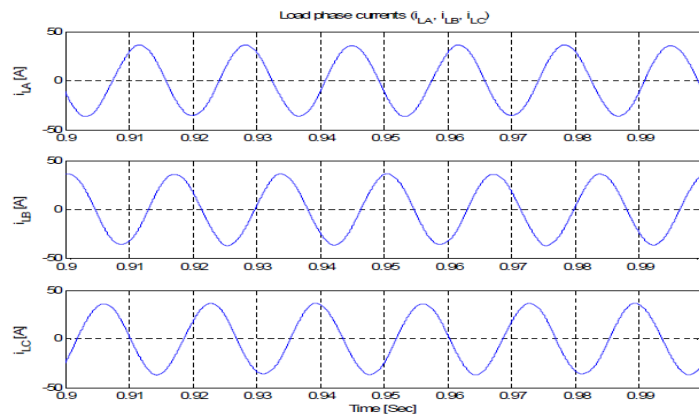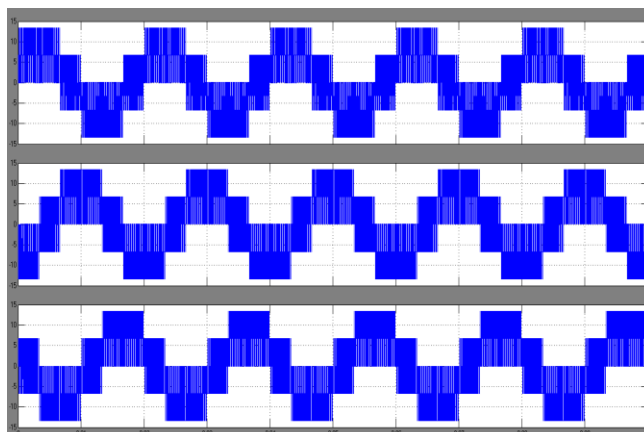**Fig.22** Simulation results of load phase currents (iLA, iLB, iLC)

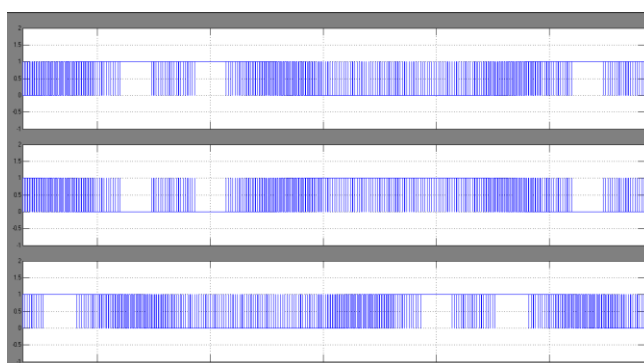**Fig. 23** Shows Inverter output phase voltage

Fig.24 shows simulation results of switching signals

VI. CONCLUSION

In this paper, a theoretical study concerning the application of the SVPWM control strategy on the buck-boost voltage source inverter was presented. The obtained simulation results were satisfactory.

The SVPWAM control method preserves the following ad-vantages compared to traditional SPWM and SVPWM method.

1) The switching power loss is reduced by 90% compared with the conventional SPWM inverter system.
2) The power density is increased by a factor of 2
3) The output voltage is about 15% more in case of SVPWM as compared to SPWM.
4) The cost is reduced by 30% because of reduced passives, heat sink, and semiconductor stress.

The effectiveness of the proposed method SVPWM in the contribution in the switching power losses reduction and to show the advantage of buck-boost voltage source inverters that carry out voltages with fewer harmonics content's injection than other type inverters.

REFERENCES

[1]. Bin Wu, High-Power Converters and AC Drives. IEEE Press, 2006.
[2]. M.Rashid, Power Electronics Pearson Prentice Hall,3/e 2007.
[3]. B. K. Bose, Power Electronics and AC Drives. Pearson rentice Hall, 2006.
[4]. Ned Mohan, Undeland and Robbins, Power Electronics Wileyedition, 2007.
[5]. D. M. Divan and G. Skibinski, "Zero-switching-loss inverters for highpower applications," *IEEE Trans. Ind. Appl.*, vol. 25, no. 4, pp. 634–643, Jul./Aug. 1989.
[6]. W.McMurray, "Resonant snubbers with auxiliary switches," *IEEE Trans. Ind. Appl.*, vol. 29, no. 2, pp. 355–362, Mar./Apr. 1993.
[7]. J.-S. Lai, R. W. Young, Sr., G. W. Ott, Jr., J. W. McKeever, and F. Z. Peng, "A delta-configured auxiliary resonant snubber inverter," *IEEE Trans. Ind. Appl.*, vol. 32, no. 3, pp. 518–525, May/Jun. 1996.
[8]. J. S. Kim and S. K. Sul, "New control scheme for ac-dc-ac converter without dc link electrolytic capacitor," in *Proc. 24th Annu. IEEE Power Electron. Spec. Conf.*, Jun. 1993, pp. 300–306.
[9]. K. Rigbers, S. Thomas, U. Boke, and R. W. De Doncker, "Behavior and loss modeling of a three-phase resonant pole inverter operating," in *Proc. 41st IAS Annu. Meeting IEEE Ind. Appl. Conf.*, Oct. 8–12, 2006, vol. 4, pp. 1694–1701.
[10]. Dweight R. Alexander, and Stephen M. Williams. "An optimal PWM algorithm implementation in a high performance 125 kVA inverter, in Conf. Rec. IEEE APEC'93, 1993, pp.771-777.